VIRTEX-4VQ STATIC SEU CHARACTERIZATION SUMMARY

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Xilinx Radiation Test Consortium

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NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

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1 VIRTEX-4 OVERVIEW

The Xilinx Virtex-4 device is a static random access memory (SRAM)-based, in-system, re-configurable field programmable gate array (FPGA). The Virtex-4 architecture includes five major, programmable block types optimized for specific functions:

- The Configurable Logic Blocks (CLB) provide functional elements for combinatorial and synchronous logic, including configurable storage elements and cascadable arithmetic functions.
- The Digital Signal Processing (DSP) Slices provide advanced arithmetic and comparison functions, including multiply and accumulate.
- The Block Memory modules provide large 18-Kbit storage elements of true dual Port RAM.
- The Digital Clock Manager (DCM) blocks provide clock frequency synthesis and de-skew.
- The bidirectional Input/Output Blocks (IOB) have optional Single Data Rate (SDR) or Double Data Rate (DDR) registers and serializers and deserializers (SERDES) enabling support for many industry input/output (I/O) standards, plus selectable drive strengths and digitally controlled output impedance.

The radiation hardened Virtex-4 QPro®-V product line includes three sub-family architectures:

- XQR4VLX200: With more than 200,000 logic cells, the LX200 is optimized for high-density common digital logic applications.
- XQR4VSX55: The SX family provides a higher ratio of DSP to CLB logic slices optimizing this architecture for DSP intensive designs.
- XQR4VFX60: The FX family includes dual PowerPC 405 processors optimizing this architecture for embedded processing applications.

Table 1. Architecture Resources of the Virtex-4VQ Product Family

	Description	XQR4VSX55	XQR4VFX60	XQR4VLX200
CFG	Configuration Bits	15,713,449	14,896,933	44,601,149
BRAM	Block Memory Bits	5,898,240	4,276,224	6,193,152
DSP	18x18 MACs**	512	128	96
PPC	PowerPC405 Processors	-	2	-
DCM	Clock Managers	12	12	12
MGT*	High-speed Transceivers*	-	N/A	-
IOBs	Input/Output Blocks	640	576	960

Notes: Only real bits in the Configuration Bit Stream that are used as control signals are counted here.
*MGTs are not supported for QPRO Virtex-4VQ Devices;
 **MAC=multiply-and-accumulate block for digital signal processing.

These QPro-V (or QV) devices are a select subset of their counterparts in the commercial Virtex-4 family with a few differences—they are intentionally fabricated on thin epitaxial wafers from a frozen mask, offered in more reliable packages, and backed by Defense Supply Center Columbus (DSCC) standards for reliability and radiation characterization

data. Like their commercial counterparts, they are fabricated in a 90-nm process geometry and are currently the most highly scaled complementary metal oxide semiconductor (CMOS) technology offered to the aerospace community.

This report is the result of the combined efforts of members within the Xilinx Radiation Test Consortium (XRTC), sometimes known as the Xilinx SEE Test Consortium. The XRTC is a voluntary association of aerospace entities, including leading aerospace companies, universities and national laboratories, combining resources to characterize reconfigurable FPGAs for aerospace applications. Previous publications of Virtex-4 radiation results are for commercial (non-epitaxial) devices; see, for example, Refs. 1–4. A notable exception is Ref. 5, which presents XRTC upset measurements of storage elements in the PowerPC405s in the XQR4VFX60. This report of upset susceptibility to heavy ions and protons of the static memory elements in the Virtex-4QV family is a direct parallel to the XRTC report on the thin epitaxial devices in the Virtex-2 family released four years ago [6].

2   LATCHUP TESTING

The QPRO Virtex-4 was tested for Single Event Effect (SEE)-induced latchup events at the Texas A&M Cyclotron Institute in March and August of 2007. There were no latchup events recorded for the XQR4VSX55-FF1148, XQR4VFX60-FF1152, and XQR4VLX200-FF1513 epitaxial devices used in those tests.

Table 2 provides a summary of the device under test (DUT) test parameters for the latchup irradiations. Each DUT was heated to a nominal pretest temperature of +120°C and biased with specification-maximum voltages.

Table 2. Latchup Test DUT Conditions

Parameter	Value	Unit
Initial DUT core temperature (target)	+120	°C
Internal voltage	1.26	V
I/O voltage	2.65	V
Auxiliary voltage	2.65	V

For the purpose of this experiment, the accepted definition of a latchup was any sudden high current modes resulting from the test run that required a power cycle of the DUT in order to recover. During the test runs, the DUT core, I/O voltages, and dynamic current consumption were captured and recorded in a running log (strip chart). Maximum current triggers were set on the power supplies in the event of a latchup condition that would result in excessive current draw. Due to the high fluxes and total fluences used for the latchup testing, it was expected that the DUT would lose its programming early in the run and would likely be subject to multiple Single Event Functional Interrupt (SEFI) conditions during the run. The purpose of the experiment was to demonstrate hardware survivability and soft recovery without the need for a device power cycle. Therefore, the test procedure adopted was as follows:

1. Program and readback to verify DUT configuration memory.
2. Heat DUT to +120°C.
3. Record initial temperature, voltage, and current conditions.
4. Irradiate the DUT to at least $1\text{x}10^7$ particles/cm^2.
    a. Record DUT power and temperature conditions during irradiation run.
5. Program and readback to verify DUT configuration memory after end of irradiation.

Table 3 shows the run parameters and results for each DUT. A 15 MeV/amu Au ion beam was primarily used to deliver an effective Linear Energy Transfer (LET) > 90 MeV/mg/cm^2 to a fluence greater than $1\text{x}10^7$ particles/cm^2. Multiple test runs were conducted in order to obtain the total fluences shown in Table 3. In some cases, additional ion species were used in order to increase penetration depth.

Table 3. Texas A&M 15 MeV/amu Ion Beam Latchup Test Data

Device	ION	Effective LET (MeV/mg/cm^2)	Effective Range (μm)	Average Flux (particles/cm^2-s)	Total Fluence (particles/cm^2)	Start Temp (°C)	End Temp (°C)	Latchup Events
XQR4VSX55								
SN#A1443	Au	108.7	71.9	7.0×10^4	2.0×10^7	82	65	None
SN#3	Ho	79.4	73	7.5×10^4	2.0×10^7	120	90	None
XQR4VFX60								
SN#601	Au	90.8	45	1.45×10^4	1.2×10^7	120	73	None
SN#602	Au	90.8	75	8.42×10^4	2.0×10^7	120	88	None
XQR4VLX200								
SN#554	Au	90.3	45	2.69×10^4	1.0×10^7	100	79	None

Because Virtex-4 devices are only offered in flip-chip packaging, irradiation is done through the top or backside of the silicon substrate. In order to reach the active layer at the bottom with a high-LET, short-range heavy ion, the backside of the silicon must be thinned to less than 100 μm. Because the bottom of the silicon is solder "bumped" to a fully populated ball-grid package, there is no way to heat the device for latchup testing with an external heating element. In order to obtain the target temperature (+120°C) in vacuum, the devices were configured with a "heater" design meant to increase dynamic current consumption sufficient to heat the transistor junctions to a desired temperature. The core temperature of the device is monitored by measuring the resistance of an internal diode specifically provided for this purpose.

The heater design is a long shift-register chain of CLB flip-flops. Typically, this chain is long enough to consume more than 75% of the available device resources. The start of the register chain is fed by a one-bit counter so that alternating ones and zeros advance through the chain with each clock pulse. In order to obtain a high enough frequency to meet the dynamic consumption requirements, a DCM is used to multiply the input clock frequency. The typical internal clock frequency was ~80MHz.

Early in each irradiation, the configuration of the device was upset. Thus, the shift-register functionality is lost almost immediately due to the high flux used. Therefore, we simultaneously disabled the clock source and turned on the ion beam for each latchup run. This reduced the current consumption at the initiation of the test to static value so that current events, possibly due to latchup events, could be more closely monitored. However, as a consequence, from the moment the source clock was deactivated, the device began to cool. Table 3 notes the starting and ending junction temperatures for each test.

3   STATIC TESTING

The static single-event-upset (SEU) experimentation was performed to determine the saturation cross section and energy threshold of upsets in the configuration and block memory cells for the XQR4VSX55, XQR4VFX60, and XQR4VLX200 for both Heavy Ion and Proton. In addition, each device was carefully scrutinized for any SEFI conditions during all experiments conducted.

3.1   Experiment Set-up

Figure 1 shows the test setup in vacuum. JPL's 5-40 pin bulkhead was used to run five of the six communication cables through the vacuum chamber. The sixth was run through the 50 pin D-Sub connector provided by Texas A&M University (TAM). Three parallel cables were also sent through the 50 pin connectors (one for a DUT readback Parallel-IV cable, one for a motherboard/DUT design programming Parallel-IV cable, and one for the temperature monitoring circuit).

Figure 1. SEU Test Hardware Setup

A mounting platform with integrated power breakout cables was used for mounting the motherboard to the rotating chassis in the vacuum chamber, and for extracting the four power supplies from the 40-pin cable. The four supplies were sent through the vacuum chamber bulkhead over BNC connectors, then re-integrated to the 40-pin cable. Force and sense were tied together at the power supply (HP6629) for all four supplies, and provided the necessary 2.5V, 3.3V, and 3.3V I/O for the motherboard; the last supply was used to control heater strips attached to the back of the daughter card. The receiver/driver cards were powered by the 3.3V of the motherboard I/O. The 5V for the Parallel-IV cables and temperature sensor circuit were powered by an external Agilent E3610A, and also run through a BNC bulkhead (provided by TAM). The DUT power supply was an HP6623, which provided three supplies, with currents of 5A, 10A, and 2A on supplies one, two, and three respectively. Supply one provided 2.5V to V_{AUX} while supply two provided 1.2V to V_{INT} and supply three provided 3.3V to two V_{CCO} DUT I/O banks that talk to the motherboard. Force and sense were tied together at the bulkheads on supplies one and three (which were run through BNC bulkhead feedthroughs). High current cables were used to run force for supply two in through a 40-pin cable and bulkhead connector, and were separated back into banana cables with a second custom 40-pin connected to an additional banana cable. (20 pins were used for power and 20 for ground). Sense for supply two was sent through a BNC over banana cables and connected to force at the daughter card.

The setup for in air testing was essentially the same as in vacuum, the main exception being that the adapted connections for getting through the bulkheads were discarded. Also, USB programming cables were used via high speed hubs for the in-air irradiations.

3.2   Heavy Ion Test Results

The heavy ion testing experiments were performed at the Cyclotron Institute, TAM in March, June, and August 2007. Heavy ion test results for the XQR4VSX55, XQR4VFX60, and XQR4VLX200 are shown in Figure 2, Figure 3, and Figure 4, respectively.

The devices were tested at different incidences for an LET range of 1.2–108.7 MeV-cm^2/mg. A combination of degraders and angles were used to achieve higher LET using the same ion.

3.2.1   Configuration and Block Memory Analysis

Two designs are used to gather statistics on the Block SelectRAMs (BRAM) cross-sections. The "Half-Latch" design (developed for characterizing the recovery profile for half-latches) was used to set the initial BRAM values to all zeros; this design has almost 10% ones in the configuration memory, the most of any of our test designs. The second design, "BRAM=1," sets all BRAM cells to an initial value of ones and leaves the rest of the configuration memory unused (all zeros).

The method for collecting this data was to first run with a relatively low flux (~1x10^3 ions/cm^2·second), until there were enough upsets to get solid statistics (on the order of a few thousand). While irradiating the device, no readbacks or scrubs were initiated and SEFI detection was off. The Functional Monitor held the DUT in reset to ensure a completely static state. After irradiation, a single readback was performed by the Configuration Monitor, and the CLB and BRAM upsets were recorded. The bit stream was then readback by iMPACT and the corrupted bit stream stored for later analysis.
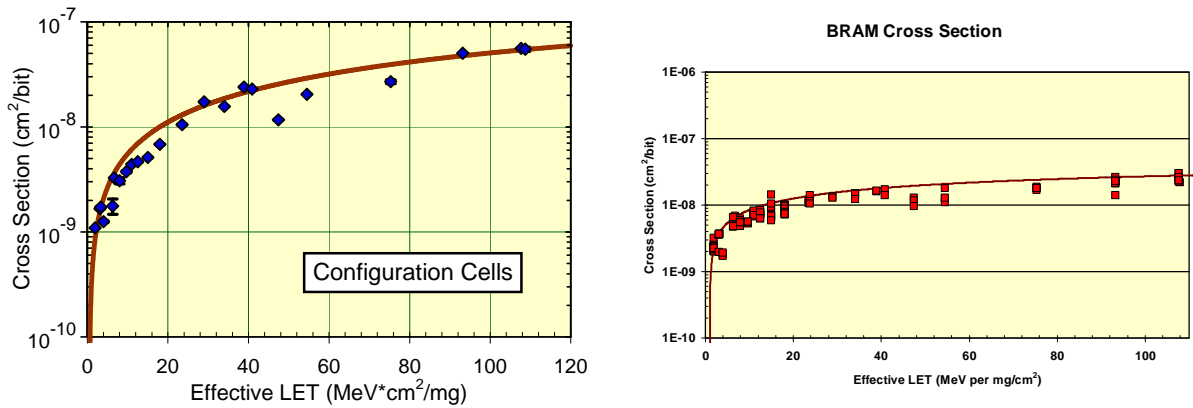
Figure 2. XQR4VSX55—Measured Main Heavy-Ion Upset Susceptibilities
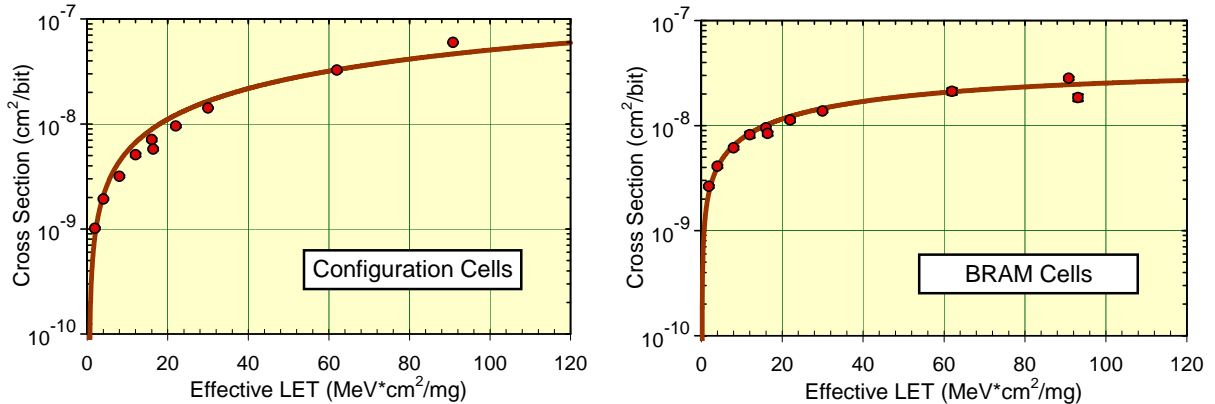
Figure 3. XQR4VFX60—Measured Main Heavy-Ion Upset Susceptibilities
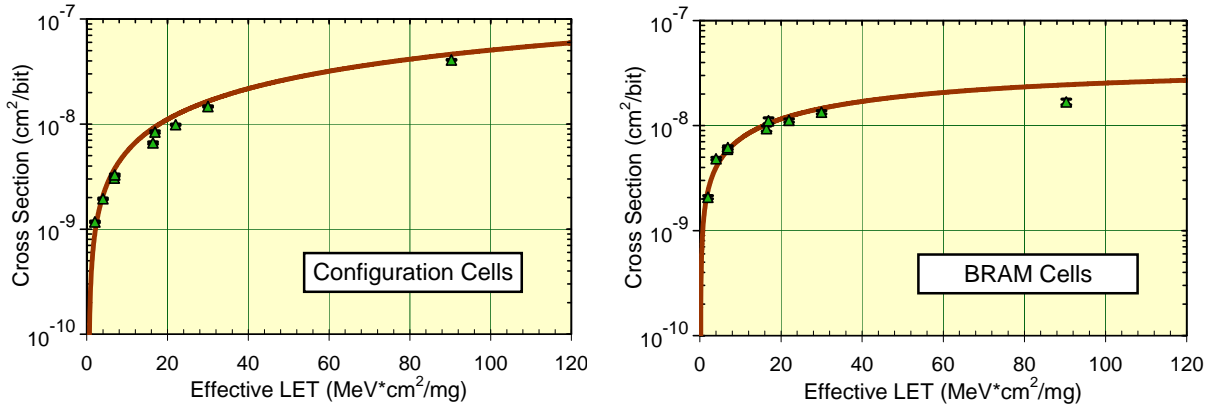
Figure 4. XQR4VLX200—Measured Main Heavy-Ion Upset Susceptibilities

The data graphs shown in this report all have two sigma statistical error bars plotted; however, in all but a few low LET cases, the configuration and BRAM data have error bars that are smaller than the plotting symbol (and thus don't show in the plots).

The SX55 static heavy ion SEU response data set has been fit with a Weibull curve function to facilitate Orbital Rate Calculations. The equation below shows this function.

$$\sigma(LET) = \sigma_{sat}(1 - \exp\{-[(LET - L_{th})/W]^S\})$$

σ_{sat} is the limiting or plateau cross section (or "limit"),

L_{th} is the LET threshold parameter (or so called "onset"),

W is the width parameter, and

S is a dimensionless exponent dubbed "power."

The data for the other devices is consistent with SX55 Weibull fit when cross sections are per-bit; see Table 4 below where the fit parameters are given.

Table 4. Virtex-4 Family Weibull Fit Parameters for
Static Memory-Cell Heavy-Ion SEU Response

Cells	Weibull Parameters			
	Limit (cm^2/bit)	Onset (MeV-cm^2/mg)	Width -	Power -
Configuration bits	2.5e-7	0.5	400	0.985
Block Memory	3.5e-8	0.2	70	0.724
User Flip-flops(0)	6.1e-7	1.5	400	0.923

As shown in Figures 2, 3, and 4, the devices exhibited upsets starting at an LET of approximately 1 MeV-cm²/mg, for both the configuration memory and the block memory cells. The saturation cross sections of the configuration memory, and block memory cells, were found to be approximately 4.37E-8 cm^2/bit and 4.19E-8 cm^2/bit, respectively.

3.2.2 *Single Event Functional Interrupt (SEFI) Analysis*

In addition to the upset susceptibility of the configuration and BRAM bits, the DUT is susceptible to SEFIs, which are caused by SEU(s) within control logic elements. The device's sensitivities to such events have been measured, and those results are presented in the next sub-section.

Typically, SEFIs are low in occurrence and are almost never seen while in orbit. However, in test environments where event rates are hugely accelerated in order to obtain statistical significance and accurate measurements of events even with negligible cross-sections, SEFIs may be observed. The criterion for a SEFI is that it requires either a complete reconfiguration or power-cycle of the device before returning to normal operation.

The observed SEFIs for the Virtex-4 are placed into six categories:

1. Power-On-Reset (POR) SEFI
2. SelectMAP (SMAP) SEFI
3. Frame Address Register (FAR) SEFI
4. Global Signal SEFI
5. Readback SEFI
6. Scrub SEFI

The POR SEFI results in a global reset of all internal storage cells and the loss of all program and state data. Observation of this mode was noted by the DONE pin dropping low, a sudden decrease of the DUT current to its starting value, an unusually large readback error count, and loss of all configured functions.

The SMAP SEFI is the loss of either read or write capabilities through the SelectMAP port. This SEFI is indicated either by the retrieval of only meaningless data or inability to refresh data. In a few cases, the port could be re-activated by using the Joint Test Action Group (JTAG) port to find and correct errors in the control registers. In the remaining occurrences, a complete reconfiguration was required to regain full port access and functions.

The FAR SEFI results in the frame address register continuously incrementing uncontrollably. It is detected by an inability to write and read control values to the FAR while all other aspects of the SelectMAP port are still fully functional. For the purpose of orbital error rate calculations, the FAR SEFI is considered a sub-set of SMAP SEFI modes. However, for characterization purposes, it is individually scrutinized.

The Global Signal SEFI was separated from other design-disrupting SEFIs for the first time in these tests. These signals include GSR (Global Set/Reset), GWE_B (Global Write Enable), GHIGH_B (Global Drive High), and others. They can all be observed through the status (STAT) register or the control (CTL) register. Some of them can be scrubbed, but others require a reconfiguration.

Readback SEFIs occur when a portion of the readback data has been upset and cannot be corrected. This condition is caused by the use of the GLUTMASK, which enables the use of SRL16s in conjunction with partial re-configuration. If GLUTMASK is not invoked then this condition does not occur. Although these bits do not affect the operability of the configured design, this condition will cause a false-positive detection of a SMAP (cyclic redundancy check [CRC] error sub-type) SEFI in the SEFI detection algorithm because the upset bits cannot be corrected through partial reconfiguration.

Scrub SEFIs were observed for the first time in this testing. They seem to be the result of an upset causing corruption of the data stream being scrubbed into the DUT. This obviously disrupts the design operation and may be accompanied by some large currents when the power supplies are set up to deliver large currents (or, alternatively, voltage sags low enough to trigger the DUT's internal power-on reset function). This is the only

SEFI that has ever been observed to have a design dependence and has been the subject of extra testing by the Consortium; more information on the Scrub SEFI will be reported elsewhere.

The selected parameters to draw the Weibull curves are given in Table 5, and the cross section curves for the major SEFI modes are displayed in the following graphs of Figure 5. Note that data for the Global Signal SEFI for the SX55 was taken before our methodology matured and only encompasses a subset of the appropriate signals; thus, the Weibull is fitted to the data of the other two part types. Otherwise, the data is consistent with the premise that SEFIs are a device-level response that is independent of die size.

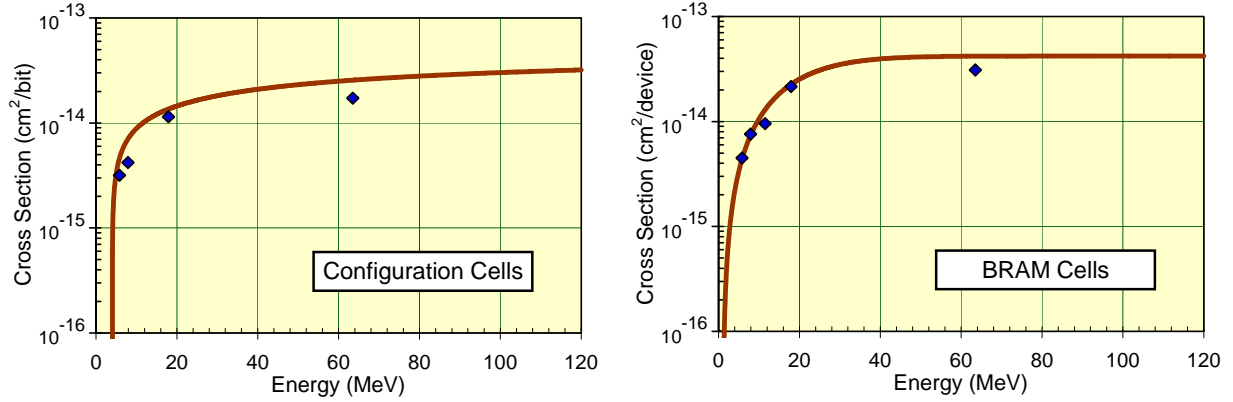**Table 5.** Weibull Fit Parameters for Virtex-4 Heavy Ion SEFIs

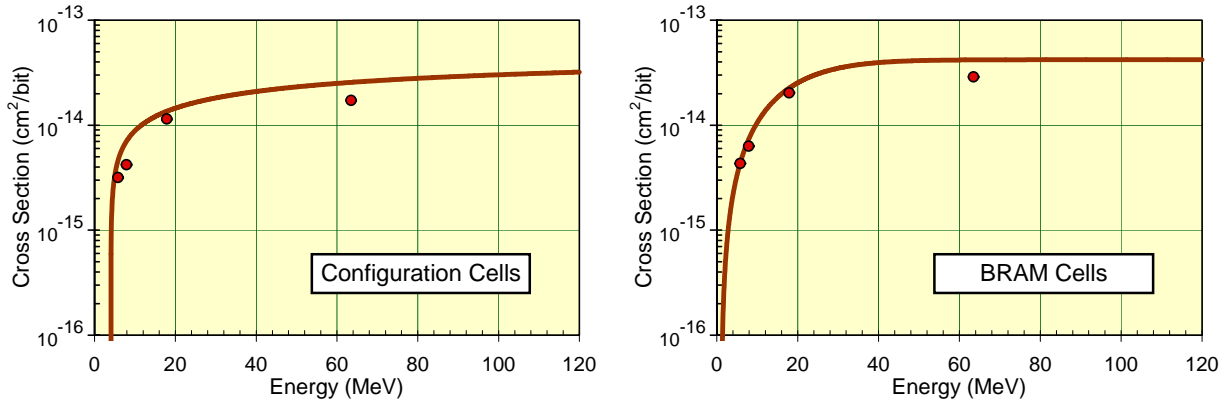| SEFI type | Weibull Parameters | | | |
	Limit (cm^2/device)	Onset (MeV-cm^2/mg)	Width -	Power -
POR-like	6.27E-06	0.2	150	1.169
SMAP	5.52E-05	0.2	1200	1.169
FAR	8.91E-07	0.2	35	1.127
Global Signal	2.01E-06	0.2	400	0.935
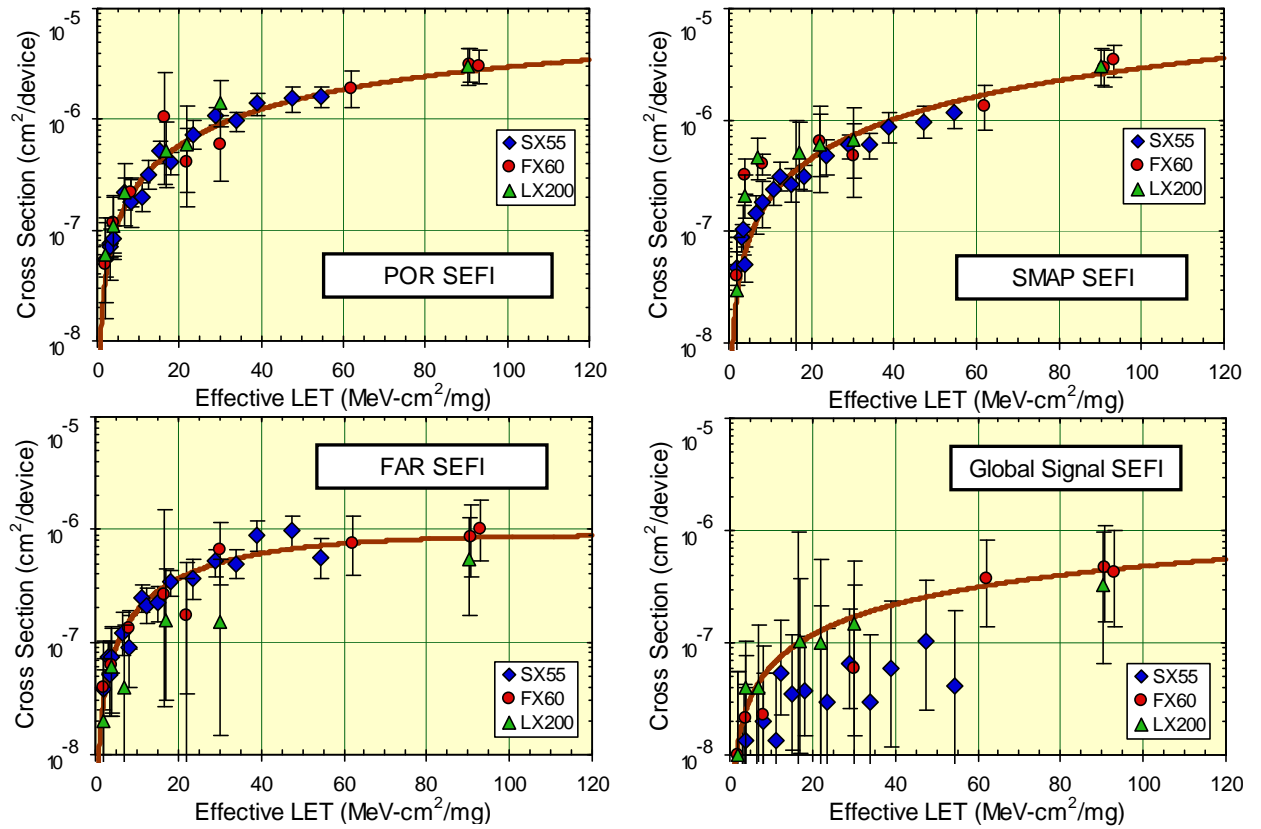
Figure 5. Virtex-4 SEFI Heavy Ion Response
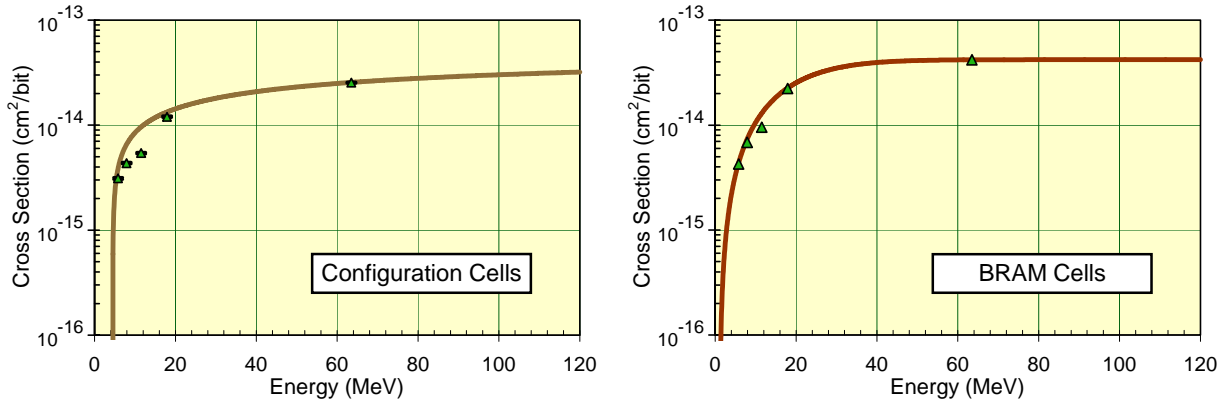
10

3.3   Proton Test Results

3.3.1   Configuration & Block Memory Analysis

Figure 6. XQR4VSX55—Measured Main Proton Upset Susceptibilities

Figure 7. XQR4VFX60—Measured Main Proton Upset Susceptibilities

Figure 8. XQR4VLX200—Measured Main Proton Upset Susceptibilities

Although not as widely used, a Weibull fit of proton data is useful as a way of describing the data in a function, so fit parameters are given in Table 6 for upsets and Table 7 for SEFIs.

Table 6. Virtex-4 Family Weibull Fit Parameters for
Static Memory-Cell Proton SEU Response

Cells	Weibull Parameters			
	Limit (cm^2/bit)	Onset (MeV)	Width -	Power -
Configuration bits	4.5E-14	4	80	0.586
Block Memory	4.5E-14	1	20	1.546

3.3.2   Single Event Functional Interrupt (SEFI) Analysis
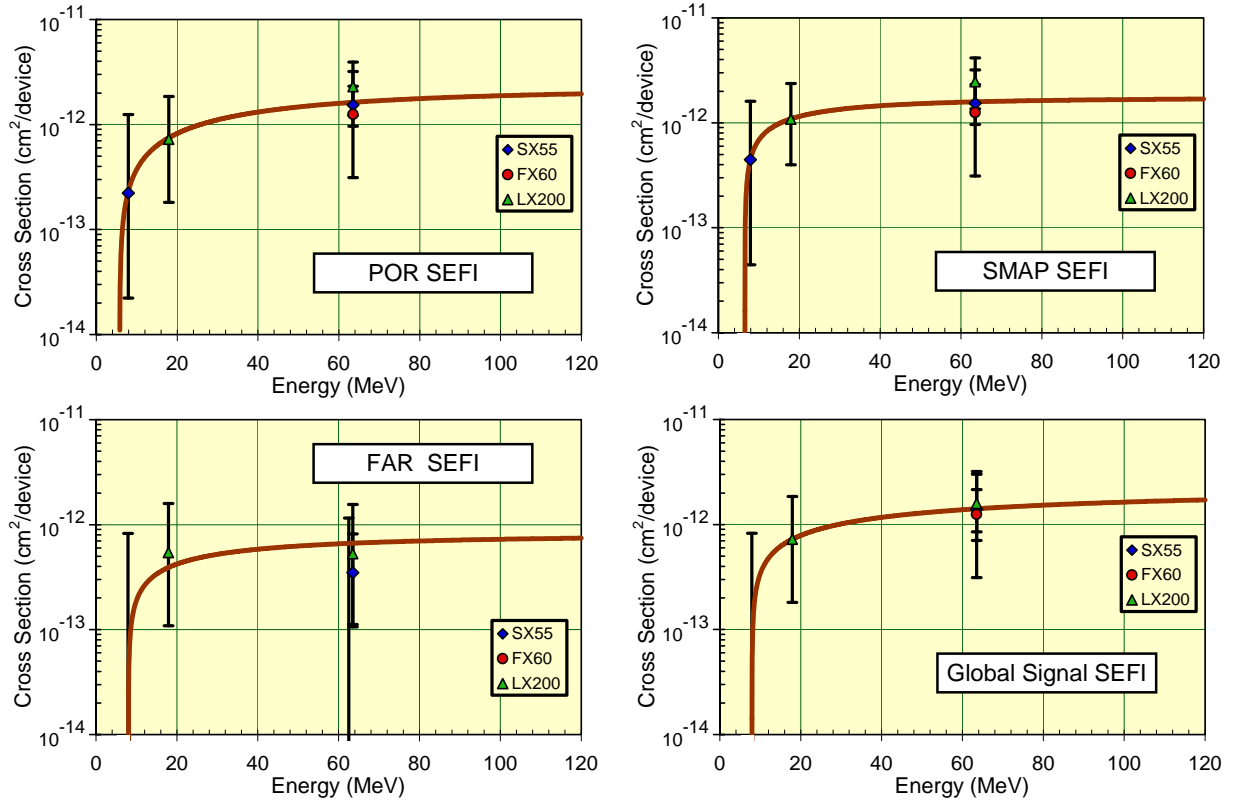
Figure 9. Virtex-4 Proton SEFI Susceptibilities

Table 7. Weibull Fit Parameters for Virtex-4 Proton-Induced SEFIs

SEFI type	Weibull Parameters			
	Limit (cm^2/device)	Onset (MeV)	Width -	Power -
POR	2.2E-12	5.8	40	0.760
SMAP	1.7E-12	6.5	10	0.568
FAR	3.3e-13	8.1	5	4.78
Global Signal	2.2E-12	7.9	55	0.545

3.4   Orbital Rate Calculations

The CREME96 (Cosmic Ray Effects on Micro-Electronic Circuits) orbital event rate estimation model provided by the Naval Research Laboratories was used to calculate orbital error rates based on the Weibull fits provided in Tables 6 and 7. The number of memory bits per device may be found in Table 1. Table 8 shows the input parameters for the CREME96 HUP and PUP files for calculating heavy ion and proton induced events, respectively. Although the SEFI data is measured in events per device, for modeling purposes, the bits per device used in CREME96 calculations are adjusted to give a relative per bit cross-section value more typical of a standard register. Even though a SEFI event may actually be caused by a logic gate transient, CREME96 models events as static upsets on a storage cell.

Table 8. CREME96 HUP and PUP parameters

CREME96 Input Parameters

Device	CFG	BRAM	POR	SMAP	GSIG	Units
SX55	15964416	5898240	10	100	4	
FX60	16726656	4276224	10	100	4	Bits per
FX140[1]	47814528	10174464	10	100	4	Device
LX200	45174756	6193153	10	100	4	
Sigma (HI)	2.50E-07	3.50E-08	6.27E-07	5.52E-07	5.03E-07	cm^2/bit
Sigma (P)	4.50E-14	4.50E-14	2.20E-13	1.70E-14	5.50E-13	
Proton (PUP)						
Onset	4	1	5.8	6.5	7.9	MeV
Width	80	20	40	10	55	w
Power	0.586	1.546	0.76	0.568	0.545	s
Limit	0.0450	0.0450	0.2200	0.0170	0.5500	$cm^2/1E-12$
Heavy Ion (HUP)						
X & Y	5.00	1.87	7.92	7.43	7.09	um
Z	1	1	1	1	1	
Onset	0.5	0.2	0.2	0.2	0.2	$MeV/cm^2/mg$
Width	400	70	150	1200	400	w
Power	0.985	0.724	1.169	1.169	0.935	s
Limit	25.00	3.50	62.70	55.20	50.25	um^2

[1]FX140 Test data will be added later.

The CREME96 orbital error rate estimates for several select orbits are shown in Tables 9a, 9b, and 9c. Calculations shown are for Quiet Solar Maximum conditions and assume 100 mils aluminum-equivalent spacecraft shielding.

Table 9a. CREME96 Calculated Orbital Upset Rates

Functional Interrupts (All Virtex-4)
Upsets/Device-Day
Typical Solar Conditions

Orbit	LEO	LEO	POLAR	CONST.	GEO
Altitude (km)	400	800	833	1,200	36,000
Inclination	51.6°	22.0°	98.7°	65.0°	0°
POR	2.83E-06	2.73E-05	1.85E-05	7.36E-05	1.21E-05
SMAP+FAR	2.25E-06	2.45E-05	1.69E-05	6.71E-05	9.46E-06
GSIG	1.57E-06	2.41E-05	1.57E-05	6.47E-05	4.87E-06
Device-Years/Event					
All SEFIs (Combined)	412	36	53	13.3	103

Table 9b. CREME96 Calculated Orbital Upset Rates

Block Memory Cells
Upsets/Device-Day
Typical Solar Conditions

Orbit	LEO	LEO	POLAR	CONST.	GEO
Altitude (km)	400	800	833	1,200	36,000
Inclination	51.6°	22.0°	98.7°	65.0°	0°
XQR4VSX55	0.92	4.02	3.14	11.1	4.49
XQR4VFX60	0.66	2.92	2.28	8.06	3.26
XQR4VFX140	-	-	-	-	-
XQR4VLX200	0.96	4.22	3.30	11.7	4.71

Table 9c. CREME96 Calculated Orbital Upset Rates

Configuration Memory Cells
Upsets/Device-Day
Typical Solar Conditions

Orbit	LEO	LEO	POLAR	CONST.	GEO
Altitude (km)	400	800	833	1,200	36,000
Inclination	51.6°	22.0°	98.7°	65.0°	0°
XQR4VSX55	0.76	7.43	5.12	20.0	4.20
XQR4VFX60	0.80	7.79	5.36	20.9	4.40
XQR4VFX140	-	-	-	-	-
XQR4VLX200	2.15	21.0	14.5	56.5	11.9

4 CONCLUSION AND FUTURE WORK

*Discussion—*QPro-V (Class-V Radiation Hardened) devices come with a guaranteed radiation specification for TID. In the case of the Virtex-4 family, that level has surpassed to 250 krad(Si) and is assured with individual wafer lot verification. The thin-epitaxial wafers are intended to reduce latchup susceptibility and the data presented here show "latchup immunity" at high bias and high temperature with the highest available LETs. Only the upset phenomena remain as potentially significant problems.

The SEFI cross sections are low enough to be almost academic (not to mention difficult to measure). For those missions where they are not low enough, it is possible to implement a dual-chip redundant system where each chip monitors the other for SEFI. In that case, it is possible to drive the system robustness to SEFIs to greater than ten nines even during a large solar flare.

The space upset rates given in Table 9 may be sufficiently low for some missions and applications, particularly those with a lot of data flushing through, where a bad pixel now and then is not a big concern. For other, more critical applications (e.g., pyrotechnic or rocket control), upset mitigation techniques may be brought to bear. In particular, full triplication of even a fairly large design is quite viable due to the large number of logic resources and pins available in these devices and due to the availability of the TMRTool software for an automated and correct mitigation of an ordinary (single-string) design.

Comparing the upset susceptibilities across Virtex generations [6], it is clear that the reduced area of the cell and increased charge sharing due to closer spacing between charge collection nodes is winning over the reduction in critical charge to upset that accompanies lower core voltage. However, while per bit rates in a given environment are going down, the growth in the number of bits more than compensates so that the device upset rates do increase with the reduction in feature sizes across the generations of FPGAs.

*Future Work—*This document focuses on summarizing the Consortium experimental results related to basic "static" cross sections for almost all memory-elements implementations that exist in the Virtex-4 family devices. These cross sections are expected to be the dominant cause of system errors in a Virtex-4 design for aerospace applications—either directly for unmitigated designs or indirectly, via the probability of coincident errors in the same section of redundant domains in TMR designs. Transients are not expected to contribute significantly. Consortium dynamic and mitigation testing will be reported separately. The dynamic testing is aimed at measuring elements like DCMs that cannot be measured in static testing. Indeed, the SEFI testing reported here is on static elements that can only be measured while some kind of design is being run. The following are other such static elements that are/will be reported separately: (a) PowerPC associated memory elements like its registers and caches are in Ref. 5 and (b) half-latch upset test results are being analyzed (but they seem to all self-recover very quickly). Two SEFIs (RB and SCRUB) are so rare that cross-section curves cannot be constructed. SCRUB SEFIs are particularly problematic since they are accompanied by high currents

and, surprisingly, the SCRUB SEFI cross section varies with design. As a result, the Consortium has spent a significant portion of several additional test trips on the SCRUB SEFI and there are identified minimization strategies (readback mostly, scrub-on-upset and/or frame-based scrubbing) that make the problem academically small.

Work remains to analyze and report on two of the smaller cross-section (and more difficult to de-convolve and count) phenomena: (1) BRAM group errors, and (2) upsets of clusters of user FFs. This report will be revised (or supplements issued) as more data are analyzed and/or additional testing brings more data to bear on these susceptibilities.

Finally, the most important remaining work is to confirm that the FX140 has susceptibilities that are consistent with the other members of the Virtex-4QV family, as reported here. While the expectation is that the per bit upset cross section vs. LET for configuration cells, BRAMs, and user flip-flops is the same across all family members, we plan to confirm this expectation with testing on the XQ4VFX140 when it becomes available later this year. Similarly, at selected LETs, per device SEFI cross sections will be measured to show consistency; alternatively, if inconsistencies are noted, SEFIs will be measured for a complete set of LETs.

Conclusion—The Virtex-4QV family of SRAM-based reconfigurable FPGAs performed well in these heavy-ion and proton irradiations, exhibiting no single-event latchup (SEL) even at elevated temperature and spec-max voltages. All three Virtex-4 family members (LX, SX, and FX) exhibited low total SEFI susceptibility to heavy ions and protons with a resulting rate of approximately one per 100 years in the geosynchronous radiation environment. Upsets of the configuration SRAM elements (as well as the user Block RAMs and the user flip-flops) are a significant concern, based on these data. While the upset rates (a few bits per day in geostationary orbit [GEO]) may be acceptable for some applications, critical applications will require design level mitigation, typically TMR to operate correctly through an upset and scrubbing to avoid the accumulation of upsets. In the case where design-level mitigation is employed, the system error rate due to upsets can be reduced to below that of the SEFI rate for even the worst-case space environments.

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